

09355516 000000

APPLICATION
FOR
UNITED STATES LETTERS PATENT

APPLICANT NAME: Dalal et al.

TITLE: **A MULTI-LEVEL ELECTRONIC PACKAGE AND
METHOD FOR MAKING SAME**

DOCKET No.: F19-98-065

INTERNATIONAL BUSINESS MACHINES CORPORATION

CERTIFICATE OF MAILING UNDER 37 CFR 1.10

I hereby certify that, on the date shown below, this correspondence is being deposited with the United States Postal Service in an envelope addressed to the Assistant Commissioner for Patents, Box Patent Application, Washington, D.C., 20231 as "Express Mail Post Office to Addressee"

Mailing Label No. EE44381848JUS

on September 22, 1998

RobinAnn Zeno

Name of person mailing paper

RobinAnn Zeno

Signature

9/22/98

Date

**A MULTI-LEVEL ELECTRONIC PACKAGE AND METHOD FOR MAKING
SAME**

BACKGROUND OF THE INVENTION

1. TECHNICAL FIELD

- 5 This invention generally relates to electronic packaging, and more specifically relates to three-dimensional packaging to package electrical devices.

2. BACKGROUND ART

- 10 The fabrication of integrated semiconductor devices involves forming a plurality of devices on a semiconductor wafer. The wafer is then divided up into a plurality of pieces called "chips" or "semiconductor dies," with each chip comprising one or more semiconductor devices. Each chip is then placed in a "package" that has external connections (generally called "pins" or "leads") to provide accesses to signals on the chip.

- 15 Many different packages for integrated circuits have been developed. One popular package is the dual in-line package (DIP). The DIP is commonly a plastic package for many commercial applications, but also comes in ceramic packages for applications that require higher operating temperature. As the number of pins on a

package were increased, new packages were developed, such as the pin grid array (PGA). A PGA package typically has rows and columns of pins in an array, and may be either plastic or ceramic as well. As the size of electronic boards continues to shrink, other packages have been developed that provide a higher density of connections in a given space.

For example, surface-mount devices have been developed that have a ceramic package (or module) with solder pads that provide connections to the integrated circuit. These solder pads may be made much smaller than the area required by a pin in prior art DIP and PGA packages, resulting in a higher connection density. These types of surface-mount technology (SMT) packages have various names such as small outline integrated circuit (SOIC), chip scale package (CSP), small outline transistor (SOT), small outline J-lead (SOJ), fine pitch ball grid array (FPBGA), and micro-ball grid array (μ -BGA).

Surface mount modules may be mounted on a variety of different types of circuit boards, circuit modules, or other substrates (referred to herein generically as a "system board"). A system board designed to receive a surface mount module typically provides landing pads that align with the landing pads on the module. Solder balls or solder bumps may be formed on either the module landing pads, the system board landing pads, or both. The surface mount module is then placed on the system board and the entire assembly is heated until the solder balls flow and form a good electrical connection between landing pads. The array of solder balls thus serve

as an interconnect mechanism between the landing pads on the module and the landing pads on the system board.

As an example of surface mount modules, ball grid array (BGA) and column grid array (CGA) chip carrier modules have used arrays of solder balls or columns
5 (sometimes referred to as cylinders) as input and output connections. In this application, the term "solder balls" will be used generically to refer to the balls, bumps, columns, cylinders or other suitable connections used as surface mount module interconnects. Generally, the array of solder balls are arranged on a dense pitch of 1.0 and 1.27 millimeters. With a dense array of solder balls covering one
10 side of the module, BGA and CGA modules can provide a large number of input and output connections to the chip in the module without using excessive space.

When the modules are connected to the system board, the modules are flipped over and placed so that the array of solder balls are aligned with the corresponding array of landing pads on the system board. The module and system board are then
15 heated, allowing the solder paste, which is screened on an array of landing pads, to melt and flow into the system board. This establishes the physical and electrical connection between the module and the system board.

Designers are attempting to put more and more packages on one system board. This is happening for several reasons. First, having all the functions on one board
20 makes the design of the system cheaper. Second, designers have become forced to

put everything on one board because the physical size of the devices they are developing are becoming much smaller. For instance, global positioning systems, which are very complex digital and analog devices, are being designed now that are hand-held. Such devices require that a large number of packages fit onto one board.

- 5 The problem that designers are facing is that they are reaching the limits of current board design in that they can pack no more packages on a single board, yet they still desire that more functionality be placed on one board. Also, by using one system board, if a customer only needs the functionality of one part of the board, the only choices the customer has are to either buy the entire board and not use part of the
- 10 functionality or buy another, completely different board.

- One solution to these problems that some designers have tried is to create multi-level packages. By using multi-level packages, the system board can be made to grow upward instead of outward. Thus, more circuits may be packed onto the same two dimensional boards. These multi-level packages generally have multiple
- 15 levels of chips, each level of chips being attached to the next level of chips through some type of connection means (SOJ, SOIC, *etc.*).

- There are several problems with multi-level chip designs. First, the multi-level designs do not readily allow for "mix and match" components. In other words, if a customer wishes to use a first company's digital signal processor (DSP) with a
- 20 different company's radio frequency (RF) electronics, the customer basically has to

make his or her own system board on which to place these various packages. This can be very expensive and time consuming.

Second, radio frequency or electrical shielding is limited or nonexistent in these multi-level packages. This limits the types of devices that can be placed in a multi-level package. Current multi-level packages that contain RF and digital devices will perform poorly because of the lack of electrical shielding between the RF and digital devices. For mixed packages, electrical shielding is very important because digital devices will generally emit electrical emissions at around the frequency of operation and at harmonics thereof. These emissions will negatively affect both RF components and, to a lesser degree, other digital components. RF components may begin to intermittently track the frequency or harmonics of the digital components. Or RF components may "add" these stray emissions to their input or output data stream, thus yielding incorrect data. In addition, RF components will generally emit their own electrical radiation. This radiation may affect the digital devices if the devices are not isolated in an insulating package, although the effect of this radiation is somewhat less than the effect of digital radiation on RF components.

There are a variety
~~There are a variety~~ of techniques used to reduce or eliminate electrical radiation between or from digital or RF components. For instance, ground planes for the two devices may be kept completely separate or are joined at only one point. In addition to this method, a well-known and respected method of reducing radiation from a device (particularly an RF device) is a Faraday shield. Faraday shields are generally

"cans" made of metal. The can is placed over sensitive components and the metal can is then grounded. The grounded metal layer of the can prevents electromagnetic emissions emitted inside the can from escaping the can. The grounded layer also prevents electrical emissions emitted outside the can from entering the inner portion.

- 5 These cans are generally grounded in several places around the can's periphery.

Current multi-level packages, however, do not allow for cans or other shielding to prevent or reduce the effects of electronic radiation. Thus, mixed digital and RF components cannot be used together in a multi-level device without having each device exposed to possible electronic radiation and its accompanying errors.

- 10 Without a way to easily join products from several vendors in an extensible, compartmentalized, three-dimensional design while allowing mixed digital and analog components having radio frequency shielding between the two types of components, system board designers will be relegated to designing new, larger boards and may have to make end products larger to fit the boards.

DISCLOSURE OF INVENTION

The preferred embodiment of the present invention provides a multi-level package, and method for making the package, that offers a small size with compartmentalized areas that can allow for radiation shielding.

- 5 The package comprises cards and interposers that are stacked upon one another to allow for small, efficient package size. In its simplest embodiment, the invention comprises two cards and an interposer interposed between the two cards. Each card is able to have packages, chips, or devices on both sides. The interposer preferably has an opening, and the combination of the interposer's opening and the
- 10 two cards form a cavity. The cavity allows for a high amount of components to be packed into a small, three-dimensional space. The interposer supports metal routing and through-hole connections and, in combination with both cards, will act like a Faraday shield. Components inside the cavity will be shielded from electromagnetic radiation emanating from outside the cavity and components outside the cavity will
- 15 be shielded from electromagnetic radiation emanating from inside the cavity. The two cards and interposer can be multi-layered and support any type of chip or package connection, including through-hole and surface mount connections.

- The foregoing and other features and advantages of the invention will be apparent from the following more particular description of the preferred embodiments
- 20 of the invention, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

The preferred exemplary embodiment of the present invention will hereinafter be described in conjunction with the appended drawings, where like designations denote like elements, and:

5 FIG. 1 shows several views of a top card in accordance with a preferred embodiment of the invention;

FIG. 2 shows several views of an interposer in accordance with a preferred embodiment of the invention;

10 FIG. 3 shows several views of a bottom card in accordance with a preferred embodiment of the invention;

FIG. 4 shows a cross-sectional view of a preferred embodiment of the present invention;

FIG. 5 shows another cross-sectional view of a preferred embodiment of the present invention;

15 FIG. 6 shows a three-dimensional view of a preferred embodiment of the present invention;

FIG. 7 shows a cross-sectional view of another preferred embodiment of the present invention; and

FIG. 8 diagrams a method for using a preferred embodiment of the present invention.

2019 RELEASE UNDER E.O. 14176

BEST MODE FOR CARRYING OUT THE INVENTION

A preferred embodiment of the present invention provides a multi-level package, and method for making the package, that offers a small size while providing compartmentalized RF and digital areas and radiation shielding for both, if shielding
5 is desired.

The package comprises cards and interposers that are stacked upon one another to allow for small, efficient package size. In a preferred embodiment, the invention comprises two cards and an interposer interposed between the two cards. Each card is able to have packages, chips, or devices on both sides. The interposer
10 preferably has an opening, and the combination of the interposer's opening and the two cards form a cavity. The cavity allows for a high amount of components to be packed into a small, three-dimensional space. The interposer supports metal routing and through-hole connections and, in combination with both cards, will act like a Faraday shield. Components inside the cavity will be shielded from electromagnetic
15 radiation emanating from outside the cavity (and vice versa). The two cards and interposer can be multi-layered and support any type of chip or package connection, including through-hole and surface mount connections.

In a preferred embodiment of the invention, each card and interposer is preferably an organic laminate card. These cards can be multi-layered and can
20 support any chip or package attachment methods, such as through-hole or surface-

mount technology (SMT) or direct-ship attachment methods, known to those skilled in the art. Digital components are preferably placed on the top of the top card. Radio frequency (RF) components are preferably placed on the bottom of the top card and on the top of the bottom card. This design allows the RF components to have the greatest amount of shielding and should shield the digital components from the RF components as well. In addition, this allows separate digital and RF ground planes. The interposer is preferably a square or rectangular, ring-shaped circuitized structure with ball grid arrays (BGAs) on both the top and bottom surfaces that connect the interposer to the bottom of the top card and the top of the bottom card. The bottom of the bottom card will generally have only a BGA, the BGA preferably being in a joint electron device engineering council (JEDEC) standard array structure to be able to join one multi-level BGA package to another multi-level BGA package. JEDEC is an association that governs standardization rules for electronic packaging.

This packaging scheme has many advantages. Because each card can be a completely separate entity containing analog and/or digital components, each card can be separately designed and tested. Yet, the two cards can be placed together to make a complete digital and RF solution for highly compact systems such as global positioning satellite (GPS) systems. Hand-held GPS systems, in particular, need both RF and digital components placed into as small a space as possible. Furthermore, each card can be sold to customers as a separate package: If the customer wants only the digital card, the customer only need buy the digital card. Components from any vendor can be used on a card and the card joined with the other card by the customer

or the distributor. For instance, if the customer chooses to use a first company's RF components with a different company's digital signal processor (DSP), this is possible. Because the package grows upward and not outward, the size of the system board can be dramatically reduced or even eliminated, or the system board's size may be kept the same and more functionality added to the board. Finally, the package allows attachment of heat sinks or other devices to the top of the package.

Turning now to FIG.s 1-6, the simplest preferred embodiment of the multi-level package is shown. FIG. 1 shows top card 110; FIG. 2 shows interposer 130; and FIG. 3 shows bottom card 150. Top card 110 and bottom card 150 are preferably circuitized cards having through-holes, landing pads, and other similar circuitized mechanisms able to interconnect electronic components to themselves and the card. FIG.s 4 and 5 show cross-sectional views of the three levels as they are preferably connected to create a single, multi-level package. FIG. 6 shows a three-dimensional view of an embodiment of the present invention. Each card supports many different types of components and connection methods for those components. The term "components" is meant to encompass any electrical device, chip, or package that can be mounted to a circuitized card in any known or to be invented manner. The components shown in FIG.s 1-6 are merely exemplary and are not meant to be limiting in any way. FIG.s 4, 5 and 6 show an embodiment of a complete package, wherein interposer 130 is interposed between, and connected to, top card 110 and bottom card 150. The connection mechanisms are preferably ball grid arrays (BGAs),

but could be any method for connecting cards or interposers known to those skilled in the art.

Interposer 130 has an opening 134 defined by inside edge 180. Inside edge 180, its corresponding opening 134, bottom surface 114 of top card 110, and the top surface 142 of bottom card 150, define a cavity 133. Cavity 133 preferably contains a multiplicity of components. These components preferably require electromagnetic shielding, and one or more grounded solder balls 182, 185, and/or 187 on interposer 130 form an electromagnetic (or Faraday) shield. Thus, cavity 133 allows for a very compact, yet three-dimensional package that can offer Faraday shielding.

Turning now to FIG. 1, FIG. 1 show three views of one card of a preferred embodiment of the present invention. FIG. 1A shows a top view of top card 110 and the various exemplary digital components on top card 110. All components shown in FIG.s 1-6 are exemplary only. Top surface 112 of top card 110 has a flash random access memory (RAM) 118, a digital signal processor (DSP) 120 and a dynamic random access memory (DRAM) 116. Flash RAM 118, DSP 120, and DRAM 116 are connected to top surface 112 through any manner known to those skilled in the art. For instance, any SMT packaging scheme such as small outline integrated circuit (SOIC), chip scale package (CSP), small outline transistor (SOT), small outline J-lead (SOJ), fine pitch ball grid array (FPBGA), and micro-ball grid array (μ -BGA), thin small outline package (TSOP), *etc.* may be used. In addition, direct chip attachment mechanisms (wire-bonding or direct chip attach by using low temperature solder

bump) or through-hole mechanisms may be used. FIG. 1A, in conjunction with FIG. 4, shows three different connection schemes. DRAM 116 is connected to top surface 112 by SOJ leads 117. The connection schemes for flash RAM 118 and DSP 120 will be discussed in reference to FIG. 4.

5 Not shown in FIG. 1 is the routing between DRAM 116, DSP 120, and flash RAM 118. These devices must be connected somehow and the routing for the metal vias between the components may be performed by any manner known to those skilled in the art, such as plated through-holes, surface laminated circuits, *etc.* Top card 110 is preferably at least a four-layer board with power, ground, and two signal
10 planes. Also not shown in FIG. 1 ^{are} the through-holes that connect top surface 112 to bottom surface 114 of top card 110. These through-holes electrically connect signals from the components on top surface 112 to components on bottom surface 114.

FIG. 1B shows the bottom surface 114 of top card 110. On bottom surface 114 of top card 110 are shown several exemplary components. Bottom surface 114
15 has real-time clock (RTC) 124, 20 megahertz (MHz) crystal 122, and power manager 126. RTC 124 has a multiplicity of leads 125, 20 MHz clock 122 has two leads 123, and power manager 126 has three leads 127. Again, these components are connected to bottom surface 114 by any method known to those skilled in the art. On the periphery of bottom surface 114 are solder balls 128 of a BGA. Underneath solder
20 balls 128 will be landing pads (not shown) that electrically connect solder balls 128 to the through-holes or metal routing or vias to which the landing pads are connected.

Not shown in FIG. 1B are the metal vias connecting RTC 124, 20 MHz crystal 122 and power manager 126 to themselves and, if necessary, to DRAM 116, flash RAM 118, and DSP 120.

- Once top card 110 has all the required components on it, the card can be tested
- 5 to ensure that it is completely functional. This testing may occur before or after solder balls 128 of the BGA on the periphery of bottom surface 114 are attached to bottom surface 114. After testing, and potentially burn-in, top card 110 should be a complete product that may be sold to customers.

- FIG. 1C shows a pick up plate 190 attached to the components on top card
- 10 110. Pick up plate 190 preferably serves several purposes. First, pick up plate 190 allows a mechanical, vacuum-run device to pick up top card 110 (and anything connected to top card 110) to place top card 110 on another surface for further processing or on a surface whereby top card 110 will be attached to another card. Second, pick up plate 190 acts as a heat sink (this is more apparent in FIG.s 4 and 5).
- 15 Finally, pick up plate 190 can be joined to an even larger or differently shaped heat sink or a heat sink with a fan attached to enhance heat reduction.

Turning now to FIG. 2, FIG. 2 shows two views of an interposer designed in accordance with a preferred embodiment of the present invention. FIG. 2A shows a top view of interposer 130 and FIG. 2B shows a bottom view of interposer 130.

- 20 Interposer 130 is preferably a multi-layer board. Referring to both FIG.s 2A and 2B,

- interposer 130 has a top surface 138, a bottom surface 136, an outside edge 182 and an inside edge 180. Inside edge 180 defines opening 134. In combination with top card 110, bottom card 150, and solder balls 128, 185, and 187, inside edge 180 defines cavity 133 (illustrated in FIG.s 4 and 5). Cavity 133 will be more particularly
- 5 described with reference to FIG.s 4 and 5. Arrayed around the periphery of top surface 138 of interposer 130, between inside edge 180 and outside edge 182, are landing pads 140. These pads will make electrical contact with, be joined with, and are aligned with solder balls 128 on the bottom surface 114 of top card 110. Arrayed around the periphery of bottom surface 136 of interposer 130, between inside edge
- 10 180 and outside edge 182, are more solder balls 185. Behind each solder ball 185 on bottom surface 138 of interposer 130 is a landing pad 140 (not shown in FIG. 2B). Solder balls 185 and landing pads 140 on the bottom surface 136 of interposer 130 can be of different sizes and locations than solder balls 128 and landing pads 140 that join interposer 130 to top card 110.
- 15 Not shown in FIG. 2 are the metal vias electrically connecting individual landing pads 140 (on either top surface 128 or on bottom surface 136) to other landing pads 140 (on either top surface 138 or on bottom surface 136). In addition, through-holes that connect landing pads 140 on top surface 138 to other landing pads 140 on bottom surface 136, or vice versa, are also not shown.
- 20 In a preferred embodiment of the invention, the arrays of solder balls form two layers of metal "cages" whereby interposer 130, the solder balls, top card 110 and

bottom card 150 will act as a Faraday or electromagnetic shield for any components placed in cavity 133. Much like the screen covering the window of a microwave oven, the cages of solder balls should prevent most radiation from entering or leaving cavity 133. To act as a Faraday shield, at least some landing pads 140 must be grounded. Preferably, the corner and middle landing pads 140 would be grounded. For an interposer that is a square, with each side being 25 millimeters (mm), grounding the corner and middle landing pads 140 will result in approximately 12mm spaces between grounded balls. It is generally known that a wavelength significantly longer than the distance between grounded areas should not be able to pass through the grounded areas (in this case, the grounded balls). Using the well known formula that the speed of light is equal to frequency times wavelength, and using 12mm as the wavelength, the frequency of radiation would be about 25 gigahertz. This result indicates that frequencies less than 25 gigahertz should be rejected by a caged structure having 12mm between each grounded ball.

- 15 Of course, this is only a simplistic estimation, because such influencing factors as the amplitude of the waveform attempting to pass through the caged structure have not been taken into account. However, the structure should provide good shielding up to a high frequency. It is recommended that the balls being grounded to create a Faraday shield be selected with approximately equal spacing
- 20 between grounded balls. If this cannot be performed, the largest space between grounded balls will be the limiting factor as to the radiation shielding capability of the package. For instance, if the package is as previously described, but one side of the

square is only grounded twice at each end of this side, then the limiting wavelength will be about 25mm. This would halve the rejected radiation frequency to about 12 gigahertz. Finally, a certain minimum number of balls must be grounded for the interposer and cage to act as a Faraday shield. Those skilled in the art should keep
5 these concepts in mind when selecting an appropriate grounding scheme.

Although interposer 130 is shown in the preferred embodiment as a square or rectangular ring, other embodiments are possible. In particular, interposer 130 may be made in panel or "window pane" form to ease manufacturing. In this manufacturing process, strips or panels that consist of multiple interposer sections are
10 made. Each interposer section is joined to another interposer section through one or more lines that may be easily broken. In the particular embodiment being described, each interposer section would be shaped like a square or rectangular ring. Layers of similarly made strips would then be laminated together until multiple interposers are developed, complete with routing. The lines between interposers are then broken and
15 each interposer is complete.

Turning now to FIG. 3, FIG. 3 shows two different views of bottom card 150. FIG. 3A shows a top view of bottom card 150, while FIG. 3B shows a bottom view of bottom card 150. Top surface 142 of bottom card 150 has the following exemplary components: 3mm 1.55MHz filter 152 with leads 153; an RF processing section 160;
20 an inductor 154 having leads 155; a 40 MHz crystal 144 having leads 145; and multiple passives 146. Passives 146 will generally be either resistors or capacitors.

RF processing section 160 is a chip attached through direct chip attachment methods to top surface 142 of bottom card 150, and RF processing section 160 includes a direct-chip attached low noise amplifier (LNA) 158 and RF signal processing IC chip 156. All other components are attached to top surface 142 of bottom card 150 through any means known to those skilled in the art.

5
10
15
20

Around the periphery of the top surface the bottom card are a multiplicity of landing pads 140. The various devices are connected together and to landing pads 140 through signal lines that run on top surface 142 of bottom card 150. Around the periphery of bottom surface 170 of bottom card 150 are more landing pads 140 that are hidden in FIG. 3B by solder balls 187. As with previous cards, through holes and/or metal vias can connect landing pads 140 (on either bottom surface 170 or top surface 142 of bottom card 150) to other landing pads 140 (also on either bottom surface 170 or top surface 142 of bottom card 150). Also, solder balls 187 and landing pads 140 can be of different sizes and of different placement than the solder balls and landing pads that ^{join} ~~point~~ interposer 130 to top card 110 and interposer 130 (see FIG.s 4 and 5) to bottom card 150. It should also be noted that solder balls 187 do not have to be peripherally placed; they could be placed in the middle of bottom card 150 or entirely cover bottom card 150.

FIG.s 4 and 5 illustrate through cross-sections A-A' and B-B' (of FIG.s 1-3), respectively, that one particular embodiment of the present invention, package 500, comprises top card 110, interposer 130, and bottom card 150. Top card 110 is

5
Cond
Solder

electrically and physically connected to interposer 130 through solder balls 128. Interposer 130 is also connected to bottom card 150 through solder balls 185. Solder balls 187 on bottom surface 170 of bottom card 150 are used to electrically and physically connect package 500 to a system board or other device (not shown). Thus, all packages and chips on top card 110 are able to be connected to other packages and chips on bottom card 150 and to a system board through landing pads 140 and solder balls. Also, FIG.s 4 and 5 illustrate that cavity 133 not only is defined by inner surface 180 of interposer 130, but also is defined by bottom surface 114 of top card 110, top surface 142 of bottom card 150, and the solder balls 128, 185, and 187. Also note that inner surface 180 of interposer 130 defines opening 134. Opening 134 is shown in FIG. 2 but is not shown in FIG.s 4 and 5 to prevent confusion. The components in cavity 133 may be on either the top surface 142 of bottom card 150, on the bottom surface 114 of top card 110, or on both. The thickness of interposer 130 can be adjusted to accommodate the height of the desired components on the top surface 142 of bottom card 150 or on the bottom surface 114 of top card 110. Cavity 133 provides for a very compact, three-dimensional package, as illustrated by FIGs. 4 and 5.

In addition, by providing one or more grounds through solder balls 128, 185, and 187, interposer 130 will act as a Faraday shield to keep electronic radiation from passing through itself. In particular, the combined package of top card 110, interposer 130, bottom card 150, and solder balls 128, 185, and 187 should prevent most electromagnetic radiation from passing into or out of cavity 133. Thus, components

in cavity 133 will be less affected by external electronic radiation generated by components outside of cavity 133. In addition, components on top surface 112 of top card 110 will be shielded from electronic radiation generated by components in cavity 133. For interposer 130 to act as a Faraday shield, one or more solder balls between
5 bottom surface 114 of top card 110 and interposer 130, between top surface 142 of bottom card 150 and interposer 130, or between bottom surface 114 of top card 110 and interposer 130 and top surface 142 of bottom card 150, should be grounded.

FIG.s 4 and 5 also illustrate the many different ways in which devices can be attached to a card. FIG. 4 shows flash RAM 118 being connected to top card 110
10 through μ -BGA 190, DSP chip 120 being connected to top card 110 through direct chip attachments (C4/tin-cap) 121, 3mm 1.55MHz filter 152 being attached through normal soldering techniques, with its leads 153 attached to bottom card 150, and RF processing section 160 being attached through direct chip attachment means (C4/tin-cap 161 and underfill 194) to bottom card 150. The direct chip attachment of
15 DSP chip 120 and RF processing integrated circuit (IC) 160 require encapsulation/underfill 192 and 194, respectively. These encapsulations/underfills generally must be cured for some time. Direct chip attachment can be C4/tin-cap solder balls, as shown in FIG. 5, or wire bonding, or any other method of directly attaching a semiconductor chip to a circuitized card. FIG. 5 shows 40 MHz crystal
20 144 attached to bottom card 150 through its large leads 145 and RTC 124 being attached to top card 110 through its leads 125.

FIG.s 4 and 5 also show pickup plate 190 being attached to the TSOP body of
DRAM 116. The means for attaching pickup plate 190 can be any means known to
those skilled in the art for attaching a plate to a package or a chip. Optionally, a
thermally conducting grease could be placed between the pickup plate 190 and DSP
chip's 120 surface to enhance thermal cooling of DSP chip 120.

FIGs. 4 and 5 illustrate that component placement for the various cards is
important. If a tall component is placed on the bottom surface 114 of top card 110,
then another tall component should not be placed on the top surface 142 of bottom
card 150 or else the two components may touch when, and if, the surfaces are
connected through interposer 130. Of course, if these components should still need to
be in their respective places on their respective cards, a taller interposer 130 may be
used to alleviate this problem.

Referring now to FIG. 6, FIG. 6 shows the previously discussed components
and cards in a complete, three-dimensional package. FIG. 6 illustrates the compact
and three-dimensional nature of package 500. Package 500, in a preferred
embodiment, has both digital and analog sections that can provide a complete,
integrated solution for handheld devices needing both RF and digital components.

Finally, it should be understood that this packaging scheme is extendible.
Should another layer of digital electronics be required, another interposer 130 (the
second interposer) and its corresponding sets of solder balls could be placed on top

surface 112 of top card 110 to join top card 110 to yet another card on top of interposer 130. Thus, this second "top" card 110 would connect components on it to the components on top card 110 through the second interposer 130. In addition, should another layer need to be added after bottom card 150, a third interposer 130
5 could be added beneath bottom card 150 to connect a second "bottom" card 150 to the first bottom card 150.

These concepts are illustrated in FIG. 7. FIG. 7 shows another cross-sectional view of package 500 where another interposer 710 has been added to join a third card 720 to package 500 to create package 700. Third card 720 is a circuitized card
10 containing pads, through-hole connections, vias and the like for interconnecting electronic components to themselves and third card 720. Interposer 710 in this example is much higher (or deeper) than interposer 130, and interposer 710 joins third card 720 to bottom card 150 through solder balls 187 and 730. Solder balls 750 allow package 700 to be joined to another package or system board. Another cavity 790 is
15 formed by an opening in interposer 710 (the opening is not numbered or shown in FIG. 7 to prevent confusion), bottom card 150, and third card 720.

On third card 720 are exemplary components capacitor 780 and transformer 760. Both capacitor 780 and transformer 760 are joined to third card 720 by through-hole pins 770 and 740, respectively. The components placed on third card 720 are
20 merely exemplary. These components could be analog or digital or mixed analog and digital. In addition, further components could also be placed on bottom surface 170

Cont.
Sub 2

of bottom card 150. Interposer 710 could be specifically grounded to act as a Faraday shield or not specifically grounded for this purpose. FIG. 7 shows the variety of different configurations that packages made in accordance with the present invention can encompass. Only this cross section (B to B') will be shown, as the cross section for A to A' is similar. What is important is that packages made in accordance with the present invention allow an extensible, three-dimensional, highly compact structure that supports a vast array of components.

Turning now to FIG. 8, FIG. 8 shows a method for making packages 500 or 700 in accordance with these preferred embodiments of the invention. Method 800 begins in step 805 when vias are routed to connect the components that will be placed on the card to each other and to landing pads 140. Generally this routing step will not be performed because the entire card will usually be constructed by a card manufacturer, and the card will already have vias on it when it is received by the manufacturer. However, the step illustrates that the card will generally have all layers, through-holes, landing pads, and other similar routing and connections to enable the proper connection of components and interposers. Interposers also need to have the correct routing formed on them or the correct through-holes formed in them. In addition, electrical connections from interposer 130 to grounds on top card 110 and/or bottom card 150 must be made to ensure that interposer 130 will act as a Faraday shield.

20140001-00000000

Once the routing and electrical connections are set up, the next step performed (step 810) is to mount components on one side of a card. Mounting the components encompasses all steps known to those skilled in the art that are necessary to mount a component. In particular, encapsulation for direct mount chips will need time to cure and more than one step may be involved in mounting a direct mount chip onto a card. For instance, there will likely need to be some type of low temperature solder flow to mount the chip onto the card. Then the encapsulation or underfill will have to be applied and cured. What is important is that chips or packages can be mounted in a variety of different ways to a card. This step also encompasses adding components to an interposer, but, because of its small size, preferably only small components such as resistors or capacitors will be added. In addition, solder balls may be placed on the card during step 810 if desired.

Once all needed components are connected to one surface of a card, the functionality of the card or interposer may be tested. This is done in step 815. This testing can take any form known to those skilled in the art, *e.g.* burning in and testing using sockets. It is also possible that the step of testing can be delayed until both sides of a card have the required components on them. If errors during testing are found (step 820 = Yes), the errors are fixed and the card is re-worked, if necessary. This repair or rework occurs in step 825. Reworking can be as complex as a complete redesign and rebuild of the card, but re-working will generally only require minor modifications to the card or interposer. If a complete redesign is necessary, step 805

will again be the first step performed. If a complete redesign is not necessary, the card will be retested, in step 815, after minor modifications have been made.

- 5 If both surfaces of the card are to have components on them, step 835 is a check to ensure that both surfaces of the card are completed. If another surface of the card needs components placed on that surface (step 835 = No), then steps 805 through 820 are performed to add the components and test the functionality of the card or interposer.

- 10 Once all cards are completed (step 835 = Yes), then the cards will generally be connected to each other. Generally, cards will not be joined until step 840 because it is much easier to test cards and/or interposers individually than after they are joined. However, if desired, step 840, wherein interposers and cards are interconnected, may be moved between steps 830 and 835. Preferably, though, all cards will be completed and have components on them before the cards are connected to interposers or other cards. In step 840, an interposer is connected to a card. As an example, top card 110
15 could be joined to interposer 130 in this step. Solder balls may be placed on the card or on the interposer during this step or solder balls may already be on the cards, having been placed there in step 810. The partial package is then tested, if desired, in step 845. If there are errors (step 850 = Yes), the package is re-worked in step 853. Generally this will be a small re-work because the cards themselves will generally
20 already have been tested in step 815.

If there are no errors (step 850 = No), completion of the package is then checked. If the package is complete in step 852 (step 852 = Yes), by having all boards and interposers connected, a pick up plate and/or heat sink can be attached to the top surface of the package in step 855. If another layer has to be added (step 852 = No), such as if interposer 130 must be connected to bottom card 150, then steps 840 to 850 will be completed to add another card or interposer to the package. Once all interposers, cards and optional heat sink/pick up plate have been added to the package, package is complete. The package may now be joined to a system board or, if desired, another package.

10 While the two cards, interposers, and system boards have been described as being joined through BGAs, any method known to those skilled in the art may be used to actually connect the cards, interposer, and system boards.

Thus, the preferred embodiment provides an apparatus and method for creating an extensible multi-level package that can have separate, shielded areas for digital and RF components. Heat dissipation is also accomplished through the use of pick up plates and/or heat sinks. This multi-level package allows the cards that make it up to be individually tested and sold, and it allows different cards from different manufacturers to be used in the same package. The preferred embodiments of the present invention allow a very compact, three-dimensional package that can house any number of components having a wide variety of attachment or connection methods.

While the invention has been particularly shown and described with reference to preferred exemplary embodiments thereof, it will be understood by those skilled in the art that variations in form and detail may be made therein without departing from the spirit and scope of the invention.

0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012
1013
1014
1015
1016
1017
1018
1019
1020
1021
1022
1023
1024
1025
1026
1027
1028
1029
1030
1031
1032
1033
1034
1035
1036
1037
1038
1039
1040
1041
1042
1043
1044
1045
1046
1047
1048
1049
1050
1051
1052
1053
1054
1055
1056
1057
1058
1059
1060
1061
1062
1063
1064
1065
1066
1067
1068
1069
1070
1071
1072
1073
1074
1075
1076
1077
1078
1079
1080
1081
1082
1083
1084
1085
1086
1087
1088
1089
1090
1091
1092
1093
1094
1095
1096
1097
1098
1099
1100
1101
1102
1103
1104
1105
1106
1107
1108
1109
1110
1111
1112
1113
1114
1115
1116
1117
1118
1119
1120
1121
1122
1123
1124
1125
1126
1127
1128
1129
1130
1131
1132
1133
1134
1135
1136
1137
1138
1139
1140
1141
1142
1143
1144
1145
1146
1147
1148
1149
1150
1151
1152
1153
1154
1155
1156
1157
1158
1159
1160
1161
1162
1163
1164
1165
1166
1167
1168
1169
1170
1171
1172
1173
1174
1175
1176
1177
1178
1179
1180
1181
1182
1183
1184
1185
1186
1187
1188
1189
1190
1191
1192
1193
1194
1195
1196
1197
1198
1199
1200
1201
1202
1203
1204
1205
1206
1207
1208
1209
1210
1211
1212
1213
1214
1215
1216
1217
1218
1219
1220
1221
1222
1223
1224
1225
1226
1227
1228
1229
1230
1231
1232
1233
1234
1235
1236
1237
1238
1239
1240
1241
1242
1243
1244
1245
1246
1247
1248
1249
1250
1251
1252
1253
1254
1255
1256
1257
1258
1259
1260
1261
1262
1263
1264
1265
1266
1267
1268
1269
1270
1271
1272
1273
1274
1275
1276
1277
1278
1279
1280
1281
1282
1283
1284
1285
1286
1287
1288
1289
1290
1291
1292
1293
1294
1295
1296
1297
1298
1299
1300
1301
1302
1303
1304
1305
1306
1307
1308
1309
1310
1311
1312
1313
1314
1315
1316
1317
1318
1319
1320
1321
1322
1323
1324
1325
1326
1327
1328
1329
1330
1331
1332
1333
1334
1335
1336
1337
1338
1339
1340
1341
1342
1343
1344
1345
1346
1347
1348
1349
1350
1351
1352
1353
1354
1355
1356
1357
1358
1359
1360
1361
1362
1363
1364
1365
1366
1367
1368
1369
1370
1371
1372
1373
1374
1375
1376
1377
1378
1379
1380
1381
1382
1383
1384
1385
1386
1387
1388
1389
1390
1391
1392
1393
1394
1395
1396
1397
1398
1399
1400
1401
1402
1403
1404
1405
1406
1407
1408
1409
1410
1411
1412
1413
1414
1415
1416
1417
1418
1419
1420
1421
1422
1423
1424
1425
1426
1427
1428
1429
1430
1431
1432
1433
1434
1435
1436
1437
1438
1439
1440
1441
1442
1443
1444
1445
1446
1447
1448
1449
1450
1451
1452
1453
1454
1455
1456
1457
1458
1459
1460
1461
1462
1463
1464
1465
1466
1467
1468
1469
1470
1471
1472
1473
1474
1475
1476
1477
1478
1479
1480
1481
1482
1483
1484
1485
1486
1487
1488
1489
1490
1491
1492
1493
1494
1495
1496
1497
1498
1499
1500
1501
1502
1503
1504
1505
1506
1507
1508
1509
1510
1511
1512
1513
1514
1515
1516
1517
1518
1519
1520
1521
1522
1523
1524
1525
1526
1527
1528
1529
1530
1531
1532
1533
1534
1535
1536
1537
1538
1539
1540
1541
1542
1543
1544
1545
1546
1547
1548
1549
1550
1551
1552
1553
1554
1555
1556
1557
1558
1559
1560
1561
1562
1563
1564
1565
1566
1567
1568
1569
1570
1571
1572
1573
1574
1575
1576
1577
1578
1579
1580
1581
1582
1583
1584
1585
1586
1587
1588
1589
1590
1591
1592
1593
1594
1595
1596
1597
1598
1599
1600
1601
1602
1603
1604
1605
1606
1607
1608
1609
1610
1611
1612
1613
1614
1615
1616
1617
1618
1619
1620
1621
1622
1623
1624
1625
1626
1627
1628
1629
1630
1631
1632
1633
1634
1635
1636
1637
1638
1639
1640
1641
1642
1643
1644
1645
1646
1647
1648
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659
1660
1661
1662
1663
1664
1665
1666
1667
1668
1669
1670
1671
1672
1673
1674
1675
1676
1677
1678
1679
1680
1681
1682
1683
1684
1685
1686
1687
1688
1689
1690
1691
1692
1693
1694
1695
1696
1697
1698
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708
1709
1710
1711
1712
1713
1714
1715
1716
1717
1718
1719
1720
1721
1722
1723
1724
1725
1726
1727
1728
1729
1730
1731
1732
1733
1734
1735
1736
1737
1738
1739
1740
1741
1742
1743
1744
1745
1746
1747
1748
1749
1750
1751
1752
1753
1754
1755
1756
1757
1758
1759
1760
1761
1762
1763
1764
1765
1766
1767
1768
1769
1770
1771
1772
1773
1774
1775
1776
1777
1778
1779
1780
1781
1782
1783
1784
1785
1786
1787
1788
1789
1790
1791
1792
1793
1794
1795
1796
1797
1798
1799
1800
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
1812
1813
1814
1815
1816
1817
1818
1819
1820
1821
1822
1823
1824
1825
1826
1827
1828
1829
1830
1831
1832
1833
1834
1835
1836
1837
1838
1839
1840
1841
1842
1843
1844
1845
1846
1847
1848
1849
1850
1851
1852
1853
1854
1855
1856
1857
1858
1859
1860
1861
1862
1863
1864
1865
1866
1867
1868
1869
1870
1871
1872
1873
1874
1875
1876
1877
1878
1879
1880
1881
1882
1883
1884
1885
1886
1887
1888
1889
1890
1891
1892
1893
1894
1895
1896
1897
1898
1899
1900
1901
1902
1903
1904
1905
1906
1907
1908
1909
1910
1911
1912
1913
1914
1915
1916
1917
1918
1919
1920
1921
1922
1923
1924
1925
1926
1927
1928
1929
1930
1931
1932
1933
1934
1935
1936
1937
1938
1939
1940
1941
1942
1943
1944
1945
1946
1947
1948
1949
1950
1951
1952
1953
1954
1955
1956
1957
1958
1959
1960
1961
1962
1963
1964
1965
1966
1967
1968
1969
1970
1971
1972
1973
1974
1975
1976
1977
1978
1979
1980
1981
1982
1983
1984
1985
1986
1987
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
2034
2035
2036
2037
2038
2039
2040
2041
2042
2043
2044
2045
2046
2047
2048
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2060
2061
2062
2063
2064
2065
2066
2067
2068
2069
2070
2071
2072
2073
2074
2075
2076
2077
2078
2079
2080
2081
2082
2083
2084
2085
2086
2087
2088
2089
2090
2091
2092
2093
2094
2095
2096
2097
2098
2099
2100
2101
2102
2103
2104
2105
2106
2107
2108
2109
2110
2111
2112
2113
2114
2115
2116
2117
2118
2119
2120
2121
2122
2123
2124
2125
2126
2127
2128
2129
2130
2131
2132
2133
2134
2135
2136
2137
2138
2139
2140
2141
2142
2143
2144
2145
2146
2147
2148
2149
2150
2151
2152
2153
2154
2155
2156
2157
2158
2159
2160
2161
2162
2163
2164
2165
2166
2167
2168
2169
2170
2171
2172
2173
2174
2175
2176
2177
2178
2179
2180
2181
2182
2183
2184
2185
2186
2187
2188
2189
2190
2191
2192
2193
2194
2195
2196
2197
2198
2199
2200
2201
2202
2203
2204
2205
2206
2207
2208
2209
2210
2211
2212
2213
2214
2215
2216
2217
2218
2219
2220
2221
2222
2223
2224
2225
2226
2227
2228
2229
2230
22